(C) AMENDMENTS TO THE CLAIMS

Please amend the claims in accordance with the following complete listing of all claims in the application:

Claim 1 (currently amended): A programmable, single chip embedded processor system for input/output applications, comprising:

(a) a modular, ~~multiple-bit~~ multiple-bit, multithread processor core operable by at least four parallel and independent ~~application~~ processor threads sharing common execution logic segmented into a ~~multiple-stage~~ multiple-stage processor ~~pipeline, wherein said processor core is capable of having at least two states~~; pipeline;

(b) ~~a~~ an instruction execution logic mechanism engaged with said processor core for executing ~~an instruction set within said processor core~~ instructions from a built-in instruction set;

(c) a supervisory control unit, controlled by at least one of said processor ~~core~~ threads, for examining ~~said core processor~~ the processor core state and for controlling the operation of said processor core ~~processor operation~~;

(d) a memory ~~for~~ capable of storing ~~and executing~~ data comprising instructions from said instruction set ~~data~~; and

(e) a peripheral adaptor engaged with said processor core for transmitting input/output signals to and from said processor core.

Claim 2 (currently amended): A system as recited in Claim 1, wherein said processor pipeline includes an instruction fetch logic stage, an instruction decode logic stage, a multiple port register read stage, an address mode logic stage, an arithmetic logic unit for arithmetic and address calculations stage, a multiple port memory stage, a branch/wait logic ~~stage and~~ stage, and a multiple port register write stage.

Claim 3 (currently amended): A system as recited in Claim 1, wherein said processor core supports ~~"n" multiple~~ one or more additional independent groups of ~~independent~~ at least two processor threads, ~~threads by replicating said common~~ each group of processor threads being associated with an instruction execution logic mechanism and ~~said~~ a memory.

Claim 4 (original): A system as recited in Claim 1, further comprising a condition code mechanism implemented in said instruction set for detecting specific word data types.

Claim 5 (original): A system as recited in Claim 4, wherein the value of the least significant byte of a word is detected to be within a specific range.

Claim 6 (currently amended): A system as recited in Claim 1, wherein said instruction set includes a processor instruction for enabling individual program threads to ~~determine their thread identity~~ identify the particular processor threads on which they are being executed.

Claim 7 (currently amended): A system as recited in Claim 1, wherein said supervisory control unit is capable of examining, interpreting, and adjusting ~~examining and interpreting~~ the state of ~~multithread~~ the processor core ~~operation~~ for the purpose of ~~starting, stopping,~~ starting and stopping individual processor threads, and ~~and~~ modifying the state of each individual ~~multithread~~ processor ~~operation~~ thread.

Claim 8 (currently amended): A system as recited in Claim 7, further comprising a hardware ~~semaphone~~ semaphore vector engaged with said supervisory control unit for controlling multithread access to said peripheral adaptor and ~~system~~ said memory.

Claim 9 (currently amended): A system as recited in Claim 1, wherein said supervisory control unit is capable of being accessed and controlled by ~~each of said operating core processor~~ one or more controlling threads selected from the processor threads in the processor core, by using input/output instructions to control the operation of one or more processor threads.

Claim 10 (currently amended): A system as recited in Claim 9, wherein said one or more controlling ~~operating processor thread is~~ threads are programmable ~~and comprises any of the available threads~~.

Claim 11 (currently amended): A system as recited in Claim 9, wherein said one or more controlling ~~operating core processor thread is~~ threads are capable of reconfiguring the overall thread processing method of operation so that ~~other processing~~ two or more processor threads can support ~~multiple instruction multiple data processing~~ MIMD operations.

Claim 12 (currently amended): A system as recited in Claim 9, wherein said one or more controlling ~~operating processor thread~~ threads can reconfigure the overall thread processing method of operation so that ~~other processing~~ two or more processor threads can support ~~single instruction multiple data processing~~ SIMD operations.

Claim 13 (currently amended): A system as recited in Claim 9, wherein said one or more controlling ~~operating processor thread is~~ threads are capable of reconfiguring the overall thread processing method of operation so that ~~an arbitrary number of processing~~ two or more processor threads can support simultaneously ~~single instruction multiple data processing~~ SIMD operations, and two or more processor threads can support ~~multiple instruction multiple data processing~~ MIMD operations.

Claim 14 (currently amended): A system as recited in Claim 1, wherein said supervisory control unit is operable by a first processor thread ~~process~~ to start and stop the operation of another processor thread ~~process~~ and to examine and alter processor core state information in ~~single-step~~ single-step and ~~multiple-step~~ multiple-step modes of controlled operation.

Claim 15 (currently amended): A system as recited in Claim 1, further comprising an identifying bit ~~patterns~~ pattern embedded in ~~the unassigned bit fields of the machine instructions of said core processor~~ said instruction set.

Claim 16 (currently amended): A system as recited in Claim 1, wherein said memory ~~comprises internal memory for storing and executing core processor code and~~ is expandable by addition of external memory ~~engaged with~~ accessible by the system through said peripheral adaptor.

Claim 17 (original): A system as recited in Claim 1, wherein said supervisory control unit is configured as a peripheral to said processor core.

Claim 18 (original): A system as recited in Claim 1, wherein said peripheral adaptor is capable of controlling analog and digital processing functions.

Claim 19 (new): A system as recited in Claim 15, wherein said identifying bit pattern is used to identify programming code for code protection purposes.

Claim 20 (new): A system as recited in Claim 15, wherein said identifying bit pattern does not affect the operation of the instruction execution logic mechanism.

Upon entry of the present amendments, the claims pending in the application will be **Claims 1-20.**

(D) REMARKS AND ARGUMENTS

1. Amendments to the Specification

(a) In the ¶3 of the Office Action, the Examiner requested correction of any minor errors which the Applicants might be aware of in the specification. In response to this request:

- Paragraph [0021] of the specification has been amended to add a missing word ("processing"). The fact that a word was missing in this location is evident from the improper syntax of the subject sentence as it appeared in the specification as originally filed. Applicant submits that it is implicit from the logic and context of the sentence that the word "processing" or a word of similar meaning was intended.

- In the following sentence of paragraph [0021], the phrase "On average" has been replaced by the phrase "For one-word instructions" for purposes of correction and clarification. Applicants submit that this amendment does not constitute addition of new matter, as the meaning of the amended sentence is inherent in or implied by the context of paragraph [0021] as a whole. Further inferential support for this amendment, if necessary, may be found in paragraph [0029]; i.e., if two passes through the pipeline are required for a two-word instruction (as discussed in paragraph [0029], it follows that only one pass will be required for a one-word instruction.

- Obvious spelling errors have been corrected in paragraphs [0039], [0040], and [0044].

- Hyphenation has been introduced into various multiple-word adjectival phrases to clarify their meanings in accordance with standard punctuation rules, and to provide consistency with properly-hyphenated adjectival phrases in the specification as originally filed.

- Paragraph [0047] has been amended to correct the range of values of the "c" condition code (the correct range being evident from paragraph [0051]).

(b) As is readily apparent from the specification and claims as originally filed (see, for example, paragraphs [0020] through [0024] and Claims 9-13), and as will be discussed in further detail in connection with the claim amendments, the processor core of the present invention incorporates multiple *processor* threads (i.e., processor hardware) adapted for executing multiple *program* threads (i.e., application program code) in a pipelined architecture. In a number of instances, the specification as originally filed contained references simply to "threads", in reference to processor threads in some instances and program threads in other instances. To avoid confusion and to enhance understandability, references to "threads" in numerous parts of the specification have been changed to "processor threads" or "program threads" as appropriate. In other instances, the original specification referred to "thread processors", clearly with reference to processor hardware threads, and these references have been changed to "processor threads" to provide for uniformity of terminology.

2. Amendments to the Claims

Summary of Claim Amendments

Claim 1 has been generally reworded to enhance clarity of meaning, and to address issues of insufficient antecedent basis as set out in ¶9 and ¶10 of the Office Action.

Claim 1 has also been amended to include parenthetical subsection reference letters, solely to enhance readability of the claim, and not for any purpose related to patentability.

Claim 1 has also been amended to further describe the configuration of the independent processor threads of the processor core (i.e., each processor thread being dedicated to a specific data-processing task), and also to describe how the multithread processor core enables simultaneous execution of staggered multiple program threads.

Claim 2 has been amended to add indefinite articles solely for purposes of improving the syntax or grammatical correctness and readability of the claim, and not for reasons relating to patentability.

Claim 3 has been generally reworded to address the Examiner's objections on grounds of indefinite as set out in ¶5a of the Office Action.

Claim 6 and **Claim 7** have been generally reworded for clarification of meaning.

Claim 8 has been revised to correct a typographical error identified in ¶5b of the Office Action, and to address the issue of insufficient antecedent basis as set out in ¶10 of the Office Action.

Claims 9-16 have been generally reworded for clarification of meaning, including the addition of hyphenation of multiple-word adjectival phrases.

Claims 10-13, Claim 15, and **Claim 16** have been amended to address the issues of insufficient antecedent basis as set out in ¶¶11-13 of the Office Action. In **Claims 11-13,** the abbreviations "MIMD" and "SIMD" (defined in the specification as originally filed) have been substituted for the corresponding original claim language, solely for purposes of enhancing claim clarity and readability.

3. Claim Rejections on Grounds of Anticipation under 35 USC § 102

In ¶15 of the Office Action, the Examiner rejected Claim 1-3, 6-7, 16, and 17 on grounds of anticipation in view of the Parady reference (U.S. Patent No. 5,933,627). In specific connection with Claim 1, the Examiner states in ¶16 that Parady teaches *"a programmable single chip embedded processor system . . . comprising . . . [a] multithreaded processor core . . . operable by at least four parallel and independent application threads sharing common execution logic segmented into a multiple stage processor pipeline"* plus all other limitations recited in Claim 1 as originally filed.

The present amendment rewords several terms and phrases in Claim 1. Of particular note, the limitation "application threads" has been changed to "processor threads". Applicants submit that it is clear from the specification as originally filed that the invention incorporates multiple *processor* threads (i.e., processor hardware) for executing multiple *program* threads (i.e., application program code); the original specification uses the terms "processor thread" and "program thread" in various locations. However, the use of the phrase "application threads" in

Claim 1, as originally filed, may have inadvertently made this less than ideally clear, so the present amendment substitutes the phrase "processor threads" for "applications threads" in order to clarify this important feature of the invention.

Applicants respectfully submit that Claim 1 as amended is not anticipated by Parady or any other prior art reference. The present invention provides a small-scale micro-controller directed primarily for use in embedded applications, whereas the Parady invention is directed to a full-scale processor designed primarily for desktop PC, workstation, or server applications. The most fundamental distinction between Parady and the present invention is that the present invention executes multiple threads of an application program using multithreaded processor *hardware* – i.e., a multithread processor core comprising at least four independent processor threads – a feature that Parady neither teaches nor suggests.

In ¶16a of the Office Action, the Examiner suggests that Figure 3 in Parady discloses a multithreaded processor core. However, it is readily apparent from Figure 3 in Parady (as described at Col. 3, Lines 35-43) that the multithread aspect of the Parady invention is software-based rather than hardware-based as in the present invention. It is stated in ¶16a of the Office Action the Parady processor supports four threads (**102, 104, 106, and 108**), but in Applicants' submission it is clear that these threads are program (i.e., software) threads, not processor (i.e., hardware) threads as in the present invention. As clearly indicated in Claim 1 (as presently amended), the processor core of the present invention is configured as a multiple-stage processor pipeline comprising at least four independent stages, or processor threads, each of which is dedicated to a specific data-processing task (i.e., to execute a specific program thread). This architecture allows for multiple program threads to pass through the pipeline in a staggered fashion, with each processor thread executing a different program thread at any given time. This is accomplished in a *single processor core*.

In contrast, the Parady invention discloses a processor that processes multiple program threads by use of context switching; i.e., using a context switch to control which program thread is to be executed by the processor at any particular time. However, the processor core of Parady is executing *only one program thread at any given time*. In this sense, Parady merely discloses a software-based multithread processor with hardware assists (e.g., thread-switching logic 112). Unlike in the present invention, the processor core of Parady cannot process multiple program

threads simultaneously. The only way this could be accomplished in accordance with the Parady invention would be to provide multiple processor cores; i.e., one for each program thread to be executed.

The structural and functional differences between Parady and the present invention may be further appreciated by comparing the architecture illustrated in Figure 2 of the present application with that shown in Figures 1 and 3 of the Parady patent, having reference at the same time to Column 3, Lines 35-43 in Parady. In the present invention, program threads move sequentially and directly from one pipeline stage to the next, with a single instruction from each of the several program threads being executed on one of the processor threads of the processor core. In Parady, each of several program threads is supported by a separate instruction buffer (102, 104, 106, or 108). A *particular* program thread is provided to dispatch unit 28, which then provides the instructions from that particular program thread to the execution units 41. It is thus clearly apparent that the Parady processor can only support one program thread at a given time, unlike in the present invention. Thread-switching logic 112 allows for switching from one program thread to another, so Parady may in that sense be considered as having multithread capabilities, but in a sense fundamentally different from the multithread capabilities of the present invention. The present invention enables *simultaneous* execution of multiple program threads using a single processor core, whereas simultaneous execution of multiple program threads using the Parady technology would be possible only by incorporating additional processor cores such that a separate core would be dedicated to each program thread.

On the foregoing analysis, Applicants respectfully submit that the Parady reference fails to teach or suggest at least one limitation of amended Claim 1, and therefore cannot anticipate Claim 1 as amended. Moreover, since Claims 2-20 all depend either directly or indirectly from Claim 1, it automatically follows that the Parady reference cannot anticipate any of the dependent claims.

4. Claim Rejections on Grounds of Obviousness under 35 USC § 103

Summary of Obviousness Rejections in the Office Action

In ¶¶26-29 of the Office Action, the Examiner rejected Claims 4-5 on grounds of obviousness pursuant to 35 U.S.C. § 103(a), in view of Parady as applied to Claim 1, and further in view of Dickman et al. (U.S. Patent No. 4,556,951).

In ¶¶30-32, the Examiner rejected Claim 8 as being obvious in view of Parady and further in view of Miyamoto et al. (U.S. Patent No. 6,101,569).

In ¶¶33-39, the Examiner rejected Claims 11-13 as being obvious in view of Parady and further in view of Fernando et al. (U.S. Patent No. 6,272,616).

In ¶¶40-42, the Examiner rejected Claim 14 as being obvious in view of Parady and further in view of Bishop et al. (U.S. Patent No. 5,784,552).

In ¶¶43-45, the Examiner rejected Claim 15 as being obvious in view of Parady and further in view of Zammit et al. (EPO Application No. 1091292).

In ¶¶46-4, the Examiner rejected Claim 18 as being obvious in view of Parady and further in view of Wilske (U.S. Patent No. 4,155,115).

For the reasons that follow, Applicant submits that the subject matter of each of Claims 1-20, as presently amended or presented, is sufficiently different from the prior art that it would not have been obvious at the time the invention was made to a person having ordinary skill in the art of the invention.

General Principles re Obviousness

In order to establish a *prima facie* case of obviousness based on one or more prior art references, all of the following criteria (among others) must be met:[1]

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[1] *Per* MPEP § 706.02(j).

- The references must teach or suggest all limitations of the claim in question.

- There must be an express or implicit teaching, suggestion, or motivation to modify the references or combine their teachings so as to produce the claimed invention.

- There must be a reasonable expectation of success upon combining the teachings.

- Said teaching, suggestion, or motivation, and said reasonable expectation of success, must be found in the references themselves, and not in the applicant's disclosure.

Remarks Regarding Obviousness

On the basis of the remarks in the preceding section regarding claim rejections based on anticipation, Applicants respectfully submit that Claim 1 as presently amended comprises a limitation that Parady neither teaches nor suggests – namely, a processor core configured as a multiple-stage processor pipeline comprising at least four independent *processor* threads, each of which is dedicated to a specific data-processing task (i.e., to execute a specific *program* thread, thereby allowing for multiple program threads to pass through the pipeline in a staggered fashion, with each processor thread executing a different program thread at any given time. Applicants further submit that this limitation is not taught or suggested in any of the other prior art references cited in connection with the obviousness-based rejections in the Office Action. Accordingly, in the Applicants' respectful submission, one of the prerequisites for a *prima facie* case of obviousness is absent with respect to Claim 1, and it automatically follows that a *prima facie* case of obviousness has not been established with respect to Claims 2-20 as well, as Claims 2-20 are each dependent either directly or indirectly from Claim 1.

5. No New Matter

It is submitted that the present amendments introduce no new matter into the application. All subject matter contained in the application, as amended hereby, was expressly described in or is reasonably inferable from the originally-filed specification, claims, abstract, and/or drawings.

(E) CONCLUDING REMARKS

Applicant respectfully submits that the amendments presented herein have fully addressed all issues raised in the Office Action, and that the application will be in condition for allowance upon entry of the amendments. Accordingly, Applicant requests timely issuance of a Notice of Allowance.

Respectfully submitted on behalf of the Applicants, by their agent:

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